



AEC-Q100 可靠性认证报告

产品名称: CA-IF1044XX-Q1

版 本: V1.1

参考标准: AEC-Q100-REV-H

认证单位: 闾康科技（上海）检测技术股份有限公司

目录

1 概述	3
2 群族产品料号表.....	3
3 产品信息表	3
3.1 产品 Fab 基本信息.....	3
3.2 产品封装基本信息.....	3
4 产品可靠性认证计划.....	4
5 产品可靠性测试结果.....	6
6 MTBF&FIT	8
7 结论	8
附录 1 : EMC 测试结果	10
附录 2 : MSL1 前后 SAT 测试结果(SOIC8).....	11
附录 2 : MSL1 前后 SAT 测试结果(DFN8).....	12

1 概述

川土微电子产品的质量与可靠性测试是一个风险缓解过程，旨在确保设备在客户应用中的使用寿命。半导体晶圆制造工艺和封装级可靠性的评估方法多种多样，可能包括加速环境试验条件，随后降低到实际使用条件。芯片的可制造性评估包括验证稳健的装配流程，产品生产的连续性，确保供货能力。根据汽车电子委员会（AEC）标准和程序，川土微电子的产品评估符合行业标准测试方法。

2 群族产品料号表

封装	料号
SOIC8 (S)	CA-IF1044S-Q1/CA-IF1044VS-Q1
DFN8 (D)	CA-IF1044D-Q1/CA-IF1044VD-Q1

备注：根据 AEC-Q100 附录 1 规范，相同 Fab 工厂、Fab 工艺、相同的封装工厂、封装工艺生产的料号可以使用相似的通用数据进行认证。

3 产品信息表

3.1 产品 Fab 基本信息

晶圆工厂	DB HiTek
晶圆名称	ARIES
晶圆工艺	BCDXXX

3.2 产品封装基本信息

封装厂	UNIMOS	JCET-D3
测试厂	UNIMOS	JCET-D3
封装形式	SOIC8 (S)	DFN8(D)
Lead Frame	Cu	Cu
Bond wire	20um Au	20um Au
湿敏等级	MSL1	MSL1
工作温度等级	Grade 1 (-40°C - 125°C)	Grade 1 (-40°C - 125°C)

4 产品可靠性认证计划

分组	项目	参考标准	测试条件	测试数量	备注
Test Group A – Accelerated Environment Stress Tests					
A1	PC	J-STD-020 JESD22-A113	Preconditioning: (Test @ Rm) SMD only; Moisture Preconditioning for THB/HAST, AC/UHST, TC, &PTC; Peak Reflow Temp =260°C	Min. MSL = 3	
A2	THB/BHAST	JESD22-A101 JESD22-A110	THB: 85°C, 85%RH 1000hrs. (Test @ Rm/Hot) BHAST: 130°C, 85%RH 96hrs. (Test @ Rm/Hot)	3*77pcs	
A3	AC/TH/UHAST	JESD22-A102 JESD22-A118 JESD22-A101	AC: 121°C, 100%RH 96hrs. (Test @ Rm) TH: 85°C, 85%RH 1000hrs. (Test @ Rm) UHAST: 130°C, 85%RH 96hrs. (Test @ Rm)	3*77pcs	
A4	TC	JESD22-A104	TC: -65°C-150°C, 500cycles (Test @Rm/ Hot)	3*77pcs	
A5	PTC	JESD22-A105	PTC: -65°C-125°C, 1000cycles (Test @ Rm/Hot)	NA	Not Applicable
A6	HTSL	JESD22-A103	HTSL: Ta=150°C, 1000hrs (Test @ Rm/Hot)	1*45pcs	
Test Group B – Accelerated Lifetime Simulation Tests					
B1	HTOL	JESD22-A108	HTOL: Ta=125°C, Vcc=5V, 1000hrs (Test @ Rm/Cold/Hot)	3*77pcs	
B2	ELFR	AEC-Q100-008	ELFR: Ta=125°C, Vcc=5V, 48hrs (Test @ Rm/Hot)	3*800pcs	
B3	EDR	AEC-Q100-005	EDR: (Test @ Rm/Hot)	NA	Not Applicable
Test Group C – Package Assembly Integrity Tests					
C1	WBS	AEC-Q100-001 AEC-Q003	Wire Bond Shear Test: (Cpk > 1.67)	30wire from 5pcs	
C2	WBP	MIL-STD883 AEC-Q003	Wire Bond Pull: (Cpk > 1.67); Each bonder used	30wire from 5pcs	
C3	SD	JESD22-B102 JSTD-002D	Solderability: (>95% coverage) 8hr steam aging prior to testing	1*15pcs	
C4	PD	JESD22-B100 JESD22-B108 AEC-Q003	Physical Dimensions: (Cpk > 1.67)	3*10pcs	
C5	SBS	AEC-Q100-010 AEC-Q003	Solder Ball Shear: (Cpk > 1.67); 5 balls from min. of 10 devices	NA	Not Applicable
C6	LI	JESD22 B105	Lead Integrity: (No lead cracking or breaking); Through-hole only; 10 leads from each of 5 devices	NA	Not Applicable

分组	项目	参考标准	测试条件	测试数量	备注
Test Group D - Die Fabrication Reliability Tests					
D1	EM	JESD61	Electromigration		
D2	TDDDB	JESD35	Time Dependent Dielectric Breakdown		
D3	HCI	JESD60 & 28	Hot Carrier Injection		
D4	NBTI	JESD90	Negative Bias Temperature Instability		
D5	SM	JESD61, 87, & 202	Stress Migration		
Test Group E- Electrical Verification					
E1	TEST	per datasheet	Pre and Post Stress Electrical Test	all	
E2	HBM	AEC Q100-002	HBM: 500V,1KV,2KV,6KV(Test @ Rm/Hot)	3pcs/voltage level	
E3	CDM	AEC-Q100-011	CDM: 250V,500V,750V,1KV,2KV(Test @ Rm/Hot)	3pcs/voltage level	
E4	LU	AEC-Q100-004	Latch-Up: (Test @ Rm/Hot)	1*6pcs	
E9	EMC	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	1*1pcs	

5 产品可靠性测试结果

分组	项目	测试条件	测试数量	样品批次	结果
Test Group A – Accelerated Environment Stress Tests(SOIC8)					
A1	PC	MSL 1	Min. MSL = 3	149AC01	Pass
				149AC02	Pass
				149AC03	Pass
A2	BHAST	130°C, 85%RH 96hrs. Vcc=5.5V	3*77pcs	149AC01	Pass
				149AC02	Pass
				149AC03	Pass
	DPA-BHAST	DPA after BHAST 96hrs	1*10pcs	149AC01	Pass
	THB	85°C,85%RH 1000hrs, Vcc=5.5V	1*77pcs	149AC01	Pass
DPA-THB	DPA after THB 1khrs	1*10pcs	149AC01	Pass	
A3	UHAST	130°C, 85%RH 96hrs.	3*77pcs	149AC01	Pass
				149AC02	Pass
				149AC03	Pass
A4	TC	-65°C-150°C, 500/1000cycles	3*77pcs	149AC01	Pass
				149AC02	Pass
				149AC03	Pass
	DPA-TC	DPA after TC 500/1000cycles	1*10pcs	149AC01	Pass
	SAT-TC	SAT after TC 1000cycles	3*77pcs	/	Pass
A6	HTSL	Ta=150°C, 1000hrs/2000hrs	1*45pcs	149AC01	Pass
Test Group A – Accelerated Environment Stress Tests(DFN8)					
A1	PC	MSL 1	Min. MSL = 3	DJ2N1	Pass
				DJ2N2	Pass
				DJ2N3	Pass
A2	BHAST	130°C, 85%RH 96hrs. Vcc=5.5V	3*77pcs	DJ2N1	Pass
				DJ2N2	Pass
				DJ2N3	Pass
	DPA-BHAST	DPA after BHAST 96hrs	1*10pcs	DJ2N1	Pass
A3	UHAST	130°C, 85%RH 96hrs.	3*77pcs	DJ2N1	Pass
				DJ2N2	Pass
				DJ2N3	Pass
A4	TC	-65°C-150°C, 500/1000cycles	3*77pcs	DJ2N1	Pass
				DJ2N2	Pass
				DJ2N3	Pass
	DPA-TC	DPA after TC 500/1000cycles	1*10pcs	DJ2N1	Pass
	SAT-TC	SAT after TC 1000cycles	3*77pcs	All	Pass
A6	HTSL	Ta=150°C, 1000hrs/2000hrs	1*45pcs	DJ2N1	Pass

Test Group B - Accelerated Lifetime Simulation Tests					
B1	HTOL	Ta=125°C, 1000hrs, Vcc=5.5V, TTL 信号输入, F=5Mbps.	3*77pcs	DUG12227A	Pass
				DUG12227B	Pass
				DUG12227C	Pass
	HTOL-robust	Ta=125°C, 2000hrs, Vcc=5.5V, TTL 信号输入, F=5Mbps.	1*77pcs	DUG12227A	Pass
B2	ELFR	ELFR: Ta=150°C, Vcc=5.5V, 24hrs, TTL 信号输入, F=5Mbps.	3*800pcs	DUG12227A	Pass
				DUG12227B	Pass
				DUG12227C	Pass
Test Group C - Package Assembly Integrity Tests(SOIC8)					
C1	WBS	Wire Bond Shear Test: (Cpk > 1.67)	30wire from 5pcs	149AC01	Pass, CPK=2.56
C2	WBP	Wire Bond Pull: (Cpk > 1.67); Each bonder used	30wire from 5pcs	149AC01	Pass, CPK=6.04
C3	SD	Solderability: (>95% coverage) 8hr steam aging prior to testing	1*15pcs	149AC01	Pass
C4	PD	Physical Dimensions: (Cpk > 1.67)	3*10pcs	149AC01	Pass
				149AC02	Pass
				149AC03	Pass
Test Group C - Package Assembly Integrity Tests(DFN8)					
C1	WBS	Wire Bond Shear Test: (Cpk > 1.67)	30wire from 5pcs	DJ2N1	Pass, CPK=2.66
C2	WBP	Wire Bond Pull: (Cpk > 1.67); Each bonder used	30wire from 5pcs	DJ2N1	Pass, CPK=5.28
C3	SD	Solderability: (>95% coverage) 8hr steam aging prior to testing	1*15pcs	DJ2N1	Pass
C4	PD	Physical Dimensions: (Cpk > 1.67)	3*10pcs	DJ2N1	Pass
				DJ2N2	Pass
				DJ2N3	Pass
TEST GROUP D - Die Fabrication Reliability Tests					
D1	EM	Electromigration			
D2	TDDDB	Time Dependant Dielectric Breakdown			
D3	HCI	Hot Carrier Injection			
D4	NBTI	Negative Bias Temperature Instability			
D5	SM	Stress Migration			
			The Die Fabrication Reliability Tests are carried out for every fabrication site. The data, test methods, calculations and internal criteria are available to the customer upon request.		
Test Group E- Electrical Verification					
E1	TEST	Pre and Post Stress Electrical Test	all	all	Pass
E2	HBM	HBM: 500V,1KV,2KV,6KV (Test @ Rm/Hot)	3pcs/voltage level	DUG02152E	Pass 6KV class 3A
E3	CDM	CDM: 250V,500V,750V,1KV,2KV(Test @ Rm/Hot)	3pcs/voltage level	DUG02152E	Pass 2KV class C6
E4	LU	Latch-Up: (Test @ Rm/Hot)	1*6pcs	DUG02152E	Pass Class II.A
E9	EMC	Electromagnetic Compatibility (Radiated Emissions)	1*1pcs	DUG02152E	参考附录 1

注: SOIC8 封装 A&C 组测试结果使用 3 lots CA-IF1042VS-Q1 结果通用数据。

6 MTBF&FIT

支撑数据									MTBF(Hrs.)	FIT
实验温度	实验电压	实验时间	样本数量	故障数量	使用温度	使用电压	活化能 (eV)	置信度		
125°C	5.5V	2000hrs	240	0	55°C	5V	0.7	60%	9.43E+07	10.60
150°C	5.5V	24hrs	2400	0	55°C	5V	0.7	60%		

7 结论

以上测试项目遵循 AEC-Q100 测试规范，由第三方实验室阅康科技执行认证，CA-IF1044XX-Q1 系列产品满足所有相关可靠性测试要求，结果全部通过，满足可靠性测试认证要求。

重要声明

上述资料仅供参考使用，用于协助 Chipanalog 客户进行设计与研发。Chipanalog 有权在不事先通知的情况下，保留因技术革新而改变上述资料的权利。

Chipanalog 产品全部经过出厂测试。针对具体的实际应用，客户需负责自行评估，并确定是否适用。Chipanalog 对客户使用所述资源的授权仅限于开发所涉及 Chipanalog 产品的相关应用。除此之外不得复制或展示所述资源，如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，Chipanalog 对此概不负责。

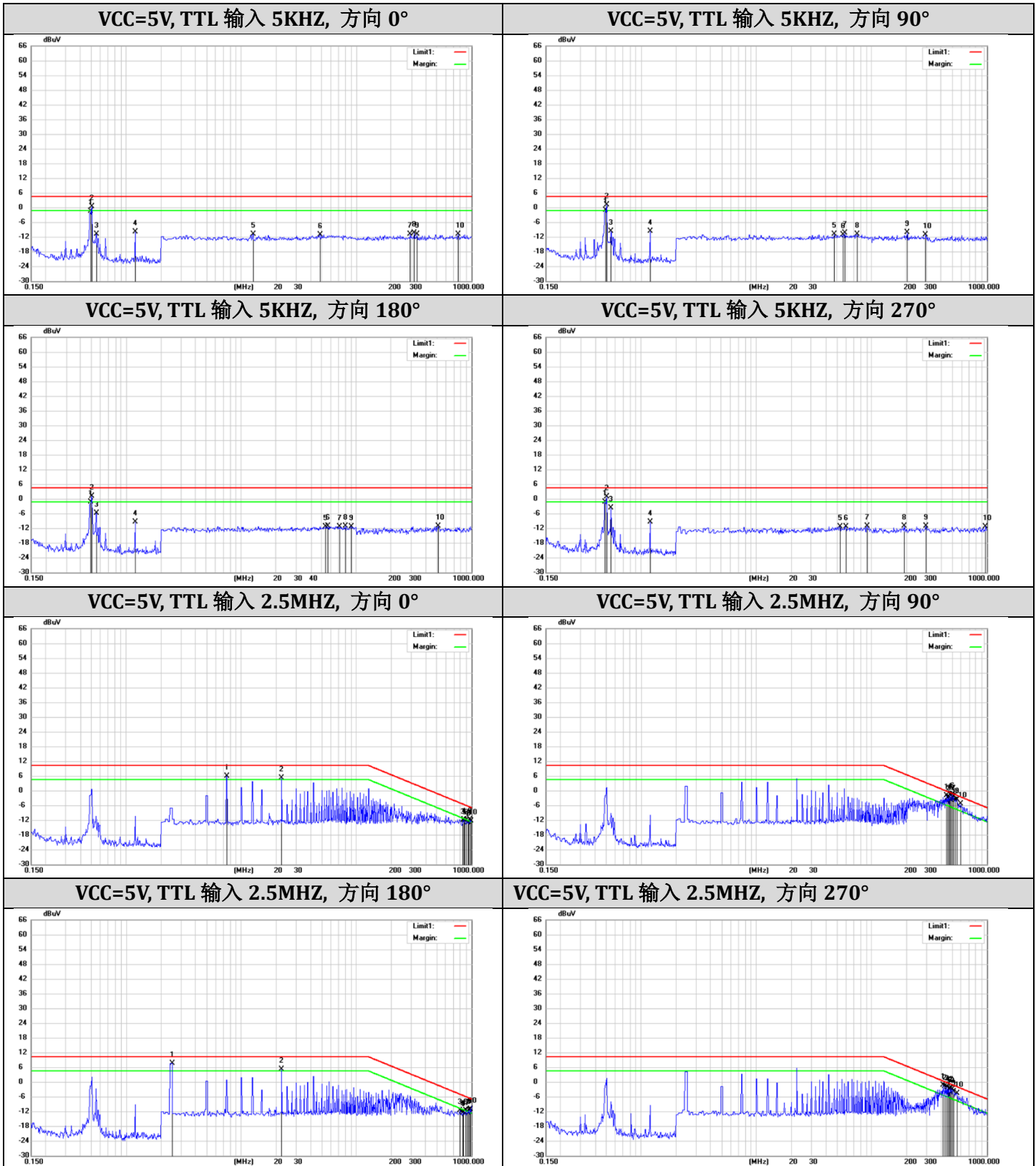
商标信息

Chipanalog Inc.®、Chipanalog®为 Chipanalog 的注册商标。

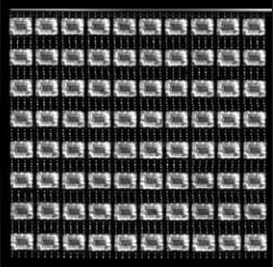
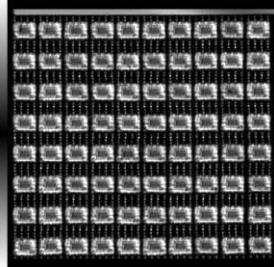
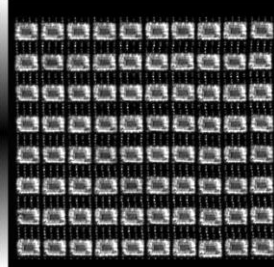
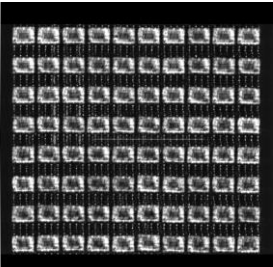
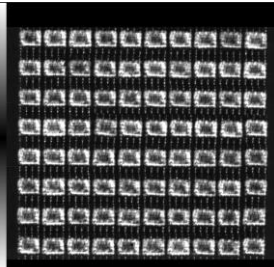
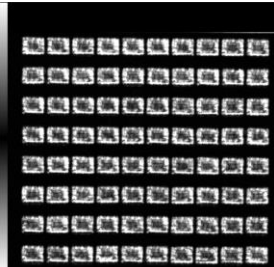
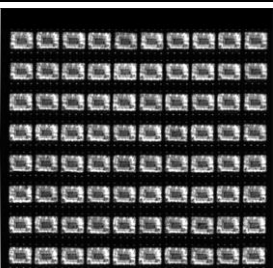
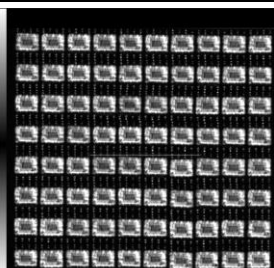
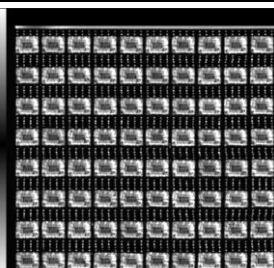
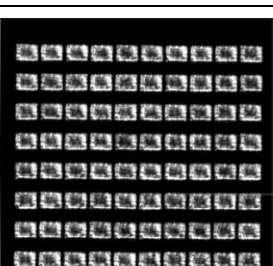
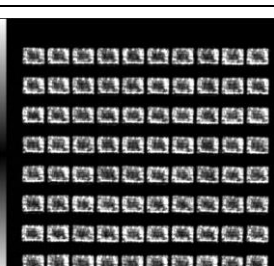
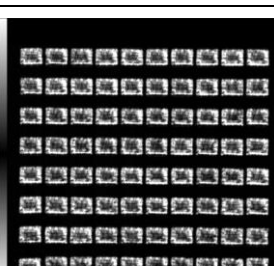
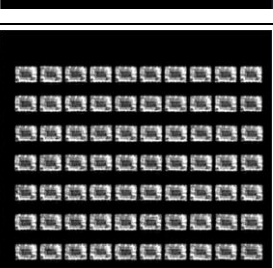
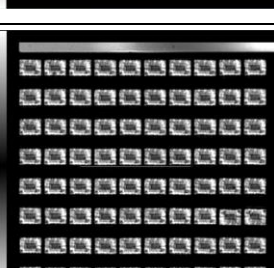
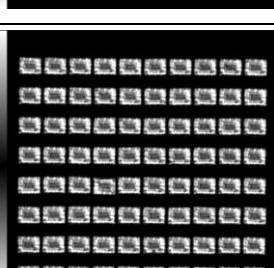
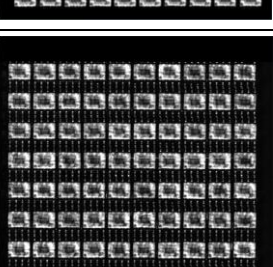
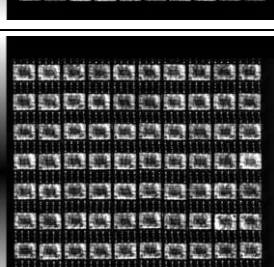
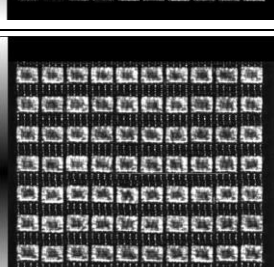
更新历史

版本	变更原因	发布日期
V1.0	初版发布	Jan. 2023
V1.1	更新鲁棒性测试结果： 1.1lot HTOL 2Khrs pass; 2.3lot TCT 1000cyc SAT&DPA*FT pass; 3.BHAST 96hrs 后 DPA pass; 4.1lot HTSL 2khrs pass.	Feb. 2023

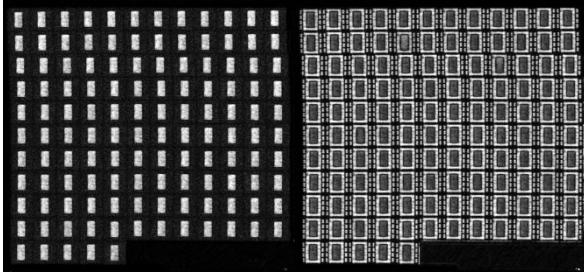
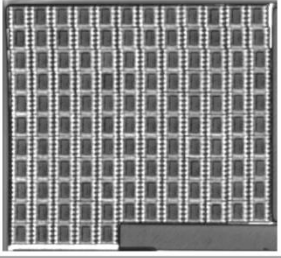
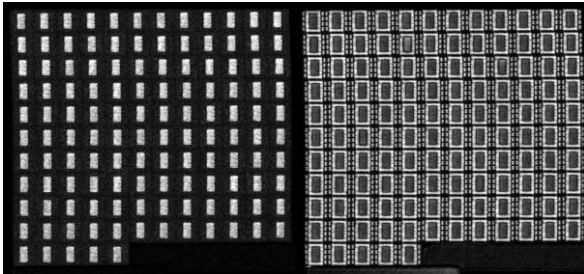
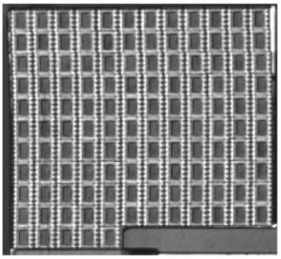
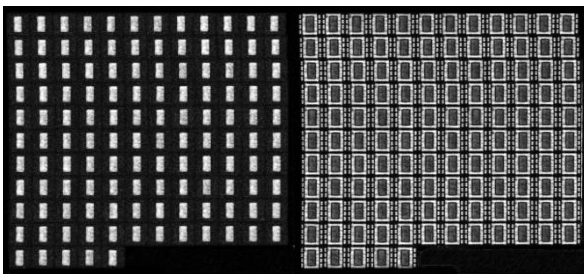
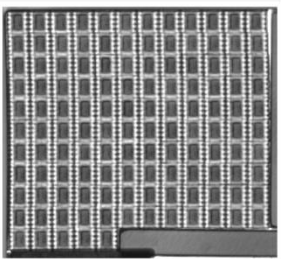
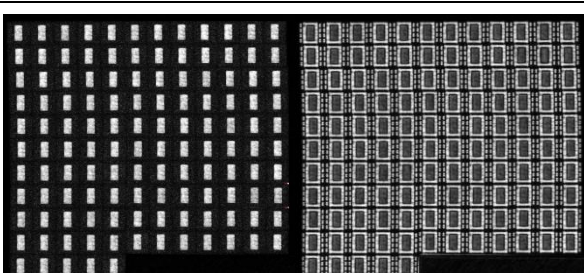
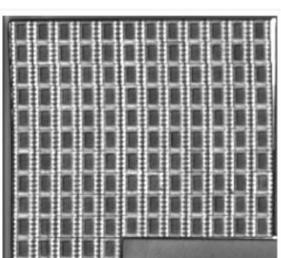
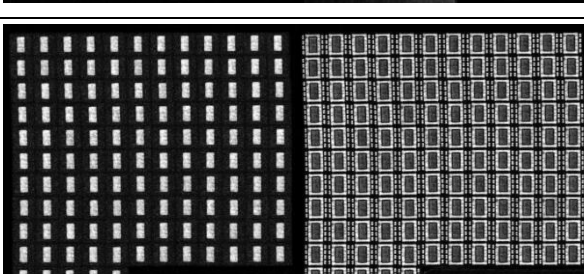
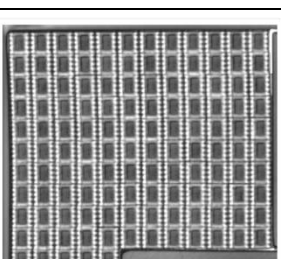
附录 1 : EMC 测试结果



附录 2 : MSL1 前后 SAT 测试结果(SOIC8)

<p>Lot 1 pre-MSL</p>					
<p>Lot 1 post-MSL</p>					
<p>Lot 2 pre-MSL</p>					
<p>Lot 2 post-MSL</p>					
<p>Lot 3 pre-MSL</p>					
<p>Lot 3 post-MSL</p>					

附录 2 : MSL1 前后 SAT 测试结果(DFN8)

<p>Lot 1 pre-MSL</p>		
<p>Lot 1 post-MSL</p>		
<p>Lot 2 pre-MSL</p>		
<p>Lot 2 post-MSL</p>		
<p>Lot 3 pre-MSL</p>		
<p>Lot 3 post-MSL</p>	